Claims

1. A semiconductor device comprising an n-channel region and a p-channel region formed on a common substrate, both channel regions having a source and a drain, the device further comprising a gate electrode common to both channel regions and spaced from the substrate by an area of non-polarising dielectric material arranged under the gate electrode.

2. A semiconductor device according to claim 1 wherein at least one of the length and/or the width of one of the channel regions differs from that of the other channel region.

3. A semiconductor device according to claim 1 or 2 wherein the gate electrode is dimensioned to have a specified ratio relative to the width and length of one of the channel regions.

4. A semiconductor device according to any one of claims 1 to 3 wherein at least one of the n-channel and the p-channel regions has a further region, arranged between either the source and/or drain regions and the channel region, having a doping concentration less than that of the source and/or drain region.

5. A semiconductor device according to any one of the preceding claims wherein an area of the substrate which separates the n-type source and n-type drain of the n-channel region, and the p-type source and p-type drain of the p-channel region has intrinsic doping only.

6. A semiconductor device according to any one of the preceding claims wherein at least one of the n-channel and p-channel regions comprises a thin film region.

7. A semiconductor device according to claim 6 wherein the thin film region comprises an organic semiconductor material.

8. A semiconductor device according to any one of claims 1 to 6 wherein the substrate comprises a thin film substrate material.

9. A semiconductor device according to claim 8 wherein the thin film substrate material comprises a direct band gap material.

10. A semiconductor device according to claim 8 or 9 wherein the thin film substrate material is supported on a transparent supporting material.

11. A semiconductor device according to claim 8 or 9, wherein the gate electrode and the non-polarising dielectric material comprise transparent materials.

12. A semiconductor device according to any one of the preceding claims wherein the substrate has a thickness arranged to enable the n-channel region and p-channel region under the gate to electrode function as fully or partially depleted regions.

13 A semiconductor device according to any one of the preceding claims wherein the source of one region is serially coupled with the drain of the other region to provide a device for functioning as an inverter.

14. A method of operating a semiconductor device according to any one of the preceding claims comprising selecting a voltage applied to the gate electrode so as to selectively switch one of the channel regions between a non-conducting and a conducting condition independently of the other channel region.

15. A method of operating a semiconductor device according to any one of claims 8 to 11 comprising operating one of the channel regions as a thin film region and coupling the source and drain regions of the other channel region to a bias voltage, thereby to alleviate

the kink effect in the said one channel region.

16. A method of operating a semiconductor device according to claim 10 or claim 11 as a light emitting device.

17. A semiconductor device according to claim 10 or 11 wherein the semiconductor device is a light emitting device.